REMARKS

CLAIMS

REJECTION OF CLAIMS 12-23, 25 and 29-34 UNDER 35 U.S.C. § 102(b)

Claims 12-23, 25 and 29-34 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,500,948 ("Hinton"). Regarding independent Claims 12, 16 and 18, the Office Action states:

> Hinton discloses a method/system of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to consolidate even and odd page frame numbers into a single page frame number field of said translation lookaside buffer;
>
> virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers
>
> comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer as **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the**

> **two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".**
>
> **For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant].**

See Office Action at pages 3-4.

Claim 12 recites "a method of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd, and consolidating even and odd page

frame number fields into a single page frame number field of said translation lookaside buffer." Claim 16 recites "a system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers." Claim 18 recites "a system to provide virtual to physical memory address translation of a translation lookaside buffer comprising a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field."

As the first point of the Applicants' argument, it was clearly indicated in the Preliminary Amendment and Request for Continued Examination dated February 22, 2007, that Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) that is recited in Claims 12 and 18. Hinton's TWB comprises elements that are functionally different from Applicants' claimed invention. For example, Hinton's TWB comprises two sets of physical registers and logical registers. Hinton's TWB is different from the system (TLB, first and second registers) recited in Claim 18. Further, Hinton's TWB does not teach the TLB recited in Claims 12 and 18. Functionally, Hinton's TWB performs write operations only; and as a consequence, it does not teach a TLB as recited in Claims 12. Therefore, for each of these reasons, Applicants respectfully submit that the system recited in Claims 12 and 18 is different from what is disclosed by Hinton. Therefore, the Applicants respectfully request allowance of the patentable subject matter recited in Claims 12 and 18.

As a second point of Applicants' argument, nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, as referenced by the Examiner, is there a teaching of "consolidating even and odd page frame numbers into *a single page frame number field*," as recited in Claim 12. Nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3 is there a teaching of "a buffer that uses a single page frame number field for storing odd/even page frame numbers," as recited in Claim 16. Nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3 is there a teaching of "buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field," as recited in Claim 18. Contrary to what the Office Action attempts to teach, Col. 6, lines 37-63 and Fig. 3 of Hinton, discloses *two* distinct and separate registers for storing "physical addresses." Thus, there is no reduction in memory provided by Hinton's invention. The Applicants request the Examiner to refer to Col. 6, lines 54-59 of Hinton which states the following:

> The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

As may be easily seen from the above passage from Hinton, Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store even numbered pages. Thus, Hinton utilizes two separate memories to store even and odd pages; as a consequence, there is *no* reduction in memory provided by Hinton. Thus, Hinton does not provide any disclosure of storing and/or retrieving even and odd page frame numbers into a "single page frame number field," as recited in independent Claim 12, using "a single page frame

number field for storing odd/even page frame numbers," as recited in Claim 16, or "using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer," as recited in Claim 18. For each of these reasons, the Applicants maintain that the Examiner has not shown a teaching of what is recited in independent Claims 12, 16, and 18, respectively. Therefore, the Applicants respectfully submit that Claims 12, 16, and 18 are in condition for allowance.

As a third point of Applicants' argument, the Office Action has improperly characterized and/or interpreted what is disclosed in Hinton. For example, at the first paragraph of page 4 of the Office Action dated 5/16/07, the Examiner states that "**Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer).**" Firstly, nowhere does Claim 12 or Claim 16 or Claim 18 recite anything about *an even or odd logical and physical address set.* Thus, for this reason alone, the Examiner has not shown a teaching of what is recited each of Claims 12, 16, and 18. Secondly, Hinton does not disclose anything about a page frame number or page frame number field as recited in Claims 12, 16, and 18. Thus, for each of these reasons alone, Hinton does not teach what is recited in Claims 12, 16, and 18; as a consequence, Claims 12, 16, and 18 contain patentable subject matter and should be allowed. The Examiner interprets the term "loaded" to mean "reading or writing" in an attempt to teach a translation lookaside buffer (TLB) recited in Claims 12 and 18. Applicants respectfully disagree that the term "loaded" is equivalent to the term "reading or writing." Therefore, the Applicants respectfully submit that for this reason alone, the Examiner has not shown a teaching of what is recited in Claims 12 and 18. Because of

each of the foregoing reasons, the Office Action does not show a teaching of what is recited in Claims 12, 16, and 18.

In summary, the Applicants respectfully submit that the Office Action does not show a teaching of each and every element recited in Claims 12, 16, and 18. Furthermore, Hinton does not teach what is recited in Claims 12, 16, and 18. The Applicants respectfully submit that independent Claims 12, 16, and 18 and their corresponding dependent claims are in condition for allowance. Applicants request that Claims 12-15, 16-17, and 18-20 should be passed to issue. Because of the arguments made with respect to the allowability of independent Claims 12, 16, and 18, the Applicants may not have commented on dependent Claims 13-15, 17, and 19-20, but reserve the right to do so in any future response, should the need arise.

Regarding new independent Claim 21, the Office Action states:

> Hinton discloses A method of implementing a reduced size translation lookaside buffet [sic] comprising:
>
> obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for writing page frame number data from said one register into said translation lookaside buffer or for reading said page frame number data from a page frame number field of an indexed entry in said translation lookaside buffer; **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-**

numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)***]

storing even or odd page frame numbers into a single page frame number field associated with said entry of said translation lookaside buffer by way of using a first storage register of said two storage registers for even page frame numbers and a second storage register of said two storage registers for odd page frame numbers when said writing is performed; **[wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)*** **wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)].**

and retrieving said even or odd page frame numbers from a single page frame number field associated with said entry of said translation lookaside buffer by way of using said first or said second storage register

when said reading is performed **["the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25)** ***(which comprises reading/retrieving from the TWB; which corresponds. to Applicant's claimed TLB)*** **wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)**

Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant].

See Office Action at pages 6-8.

Applicants have made a clarifying amendment to Claim 21. Claim 21 recites "a method comprising: obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or

b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into said single page frame number field."

The Applicants maintain that the Office Action does not show a teaching of what is recited in Claim 21. The Office Action refers to translation write buffer (TWB) registers loaded with logical and physical addresses corresponding to two sets of logical and physical registers. This is different from what is recited in Claim 21. Thus, Hinton's TWB does not teach what is recited in Claim 21. Applicants would like to point out that the Office Action states with respect to Hinton that "**Bit 12 selects which of the two entries in the TWB are to be used for this address.**" In other words, the address is to be stored in either logical register 0 or logical register 1 of Hinton's translation write buffer (TWB). Applicants' invention uses a bit "to reduce two page frame

number fields of said indexed entry into a single page frame number field." As stated by the Examiner, Hinton's invention "selects which of the two entries in a TWB are to be used for this address." Thus, Hinton's invention utilizes two entries as opposed to a single entry; as a consequence, there is no teaching or disclosure of a "bit used to reduce size of said translation lookaside buffer by way of consolidating *two* page frame number fields of said indexed entry into said *single* page frame number field," as recited in Claim 21 (emphasis denoted in italics). Furthermore, the verbiage stated by the Examiner in the Office Action is not substantiated by Hinton. For example, the Examiner states "[T]**herefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field."** From the preceding statement, the Examiner does not provide any logical reasoning as to how Hinton discloses "writing and reading even and odd page frame numbers into a single page frame number field." The Applicants do not see how referencing "an even or odd logical and physical address set" on a translation write buffer (WB) has anything to do with "writing and reading even and odd page frame numbers into a single page frame number field." Contrary to what the Office Action states, Hinton does not teach using a bit to "reduce size of said translation lookaside buffer" as recited in Claim 21. The Applicants have made a clarifying amendment to Claim 21 to obviate any interpretation issues of the patentable subject matter in Claim 21. Therefore, for each of these reasons, the Office Action does not show a teaching of Claim 21. Applicants respectfully submit that the Examiner must show a teaching of each and every element / feature of Claim 21 if she wishes to maintain this rejection. Applicants respectfully submit that Claim 21 is in

condition for allowance. Applicants respectfully submit that Claims 22-28 are in condition for allowance since these claims depend on an allowable independent Claim 21. Because of the arguments made with respect to the allowability of independent Claim 21, the Applicants may not have commented on dependent Claims 22-28, but reserve the right to do so in any future response, should the need arise.

Regarding new independent Claim 29, the Office Action states:

> Hinton discloses A method of performing a write operation using a translation lookaside buffer comprising:
>
> using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; translating a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to he used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it**

is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)***]

said indexed entry, comprising a single page frame number field used to reduce the size of said translation lookaside buffer **[With respect to this limitation, Hinton discloses "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].**

See Office Action at pages 9-10.

Claim 29 recites a method of performing a write operation using a translation lookaside buffer. As stated earlier, the Applicants had incorporated the patentable subject matter from the preamble of Claim 1, into the body of new independent Claim 29 by way of submitting a

Preliminary Amendment and Request for Continued Examination (RCE) on February 22, 2007. For this reason alone, the Applicants maintain that Claim 29 should be allowed.

Since the Office Action references the passages in Hinton that were used for Claims 12, 16, 18, and 21, the Applicants request the Examiner to refer to the arguments made for Claims 12, 16, 18, and 21. Applicants respectfully submit that the Office Action does not show a teaching of "using a bit of a virtual page number," as recited in Claim 29. For at least this reason, the Applicants respectfully submit that Claim 29 contains patentable subject matter. Furthermore, nowhere does Hinton's invention teach an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 29. Applicants maintain that Claim 29 is in condition for allowance. Furthermore, dependent Claims 30-31 are in condition for allowance since they depend on allowable Claim 29. The Applicants may not have commented on dependent Claims 30-31, but reserve the right to do so in any future response, if necessary.

Regarding new independent Claim 32, the Office Action states:

> A method of performing a read operation using a translation lookaside buffer comprising:
>
> using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether n value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page flame number field of an indexed entry of said translation 10okaside buffer, storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of

> said translation lookaside buffer **[The rationale in the rejection to claim 29 is herein incorporated].**

See Office Action at page 11.

Claim 32 recites a method of performing read operation using a translation lookaside buffer. As stated earlier, the Applicants had incorporated the patentable subject matter from the preamble of Claim 1, into the body of new independent Claim 32 by way of submitting a Preliminary Amendment and Request for Continued Examination (RCE) on February 22, 2007. For this reason alone, the Applicants maintain that Claim 32 should be allowed.

Since the Office Action references the passages in Hinton that were used for Claims 12, 16, 18, and 21, the Applicants request the Examiner to refer to the arguments made for Claims 12, 16, 18, and 21. Applicants respectfully submit that the Office Action does not show a teaching of "using a bit of a virtual page number," as recited in Claim 32. For at least this reason, the Applicants respectfully submit that Claim 32 contains patentable subject matter. Furthermore, nowhere does Hinton's invention teach an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 32. Applicants maintain that Claim 32 is in condition for allowance. Furthermore, dependent Claim 33 is in condition for allowance since it depends on allowable Claim 32. The Applicants reserve the right to comment on Claim 33 in any future response, if necessary.

Regarding new independent Claim 34, the Office Action states:

> A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:
>
> using a virtual page number stored in a first register; comparing

said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field.**

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within

> **Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant] [See figure 7 and related text].**

See Office Action at pages 11-13.

Claim 34 recites a method of probing an entry using a translation lookaside buffer. Since the Office Action references the passages in Hinton that were used for Claims 12, 16, 18, and 21, the Applicants request the Examiner to refer to the arguments made for Claims 12, 16, 18, and 21. Applicants respectfully submit that the Office Action does not show a teaching of "using a virtual page number stored in a first register," as recited in the first clause of Claim 34. For at least this reason, the Applicants respectfully submit that Claim 34 contains patentable subject matter. Applicants respectfully submit that the Office Action does not show a teaching of "comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer," as recited in the second clause of Claim 34. For at least this reason, the Applicants respectfully submit that Claim 34 contains patentable subject matter. Applicants respectfully submit that the Office Action does not show a teaching of "generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said

virtual page number, and storing said identifying number into a second register," as recited in the third and fourth clauses of Claim 34. Applicants request that the Examiner clearly disclose and identify the one or more elements of Hinton that she wishes to use to show a teaching of each and every element recited in Claim 34. Otherwise, the Examiner should withdraw her rejection to Claim 34. For at least this reason, the Applicants respectfully submit that Claim 34 contains patentable subject matter. Applicants maintain that Claim 34 is in condition for allowance.

REJECTION OF CLAIM 35 UNDER 35 U.S.C. § 103(a)

Claim 35 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art "(AAPA") in view of Hinton. Regarding independent Claim 35, the Office Action states:

> AAPA discloses A translation lookaside buffer system comprising: a translation lookaside buffer; **["TLB 104" (Applicant's Specification; Figure 1 and related text)]**
>
> a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; **"index 132" (Applicant's Specification; Figure 1 and related text)]**
>
> a second register used for storing a page size of said entry; **["page mask 136" (Applicant's Specification; Figure 1 and related text)]**
>
> a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; **["Entry Hi" (Applicant's Specification; Figure 1 and related text)]**
>
> a fourth register used for storing an even page frame number; **["entry Loo" (Applicant's Specification; Figure 1 and related text)]**
>
> and a fifth register used for storing an odd page frame number, **["entry Lol" (Applicant's Specification; Figure 1 and related text)].**

AAPA does not disclose expressly said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

Hinton discloses said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31**

of this logical address with -their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism, by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)*** **wherein "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].**

Applicant Admitted Prior Art (AAPA) and Hinton et al. (US 5,500,948) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the TLB system as taught by APPA and further said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said

> even page flame number is to be stored in said fourth register or -aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as taught by Hinton.
>
> The motivation for doing so would have been because Hinton discloses **["it is an object of the present invention to provide an address translation mechanism that will translate a logical address from a program counter to a physical address to be used to check an on-chip cache for an instruction" (Col. 1, lines 57-60) for efficient address translation]:**
>
> Therefore, it would have been obvious to combine Applicant Admitted Prior Art (AAPA) with Hinton et al. (US 5,500,948) for the benefit of creating a translation lookaside buffer to obtain the invention as specified in claims 35.

See Office Action at pages 15-18.

As stated earlier, the Applicants had incorporated the patentable subject matter from the preamble of Claim 1, into the body of new independent Claim 35 by way of submitting a Preliminary Amendment and Request for Continued Examination (RCE) on February 22, 2007. For this reason alone, the Applicants maintain that Claim 35 should be allowed.

Since the Office Action references the passages in Hinton that were used for Claims 12, 16, 18, and 21, the Applicants request the Examiner to refer to the arguments made for Claims 12, 16, 18, and 21. Further, the Applicants respectfully submit that the Office Action does not show a teaching of what is recited in the fifth clause of Claim 35. For example, the Office Action does not show a teaching of "wherein use of said single page frame number field reduces

the size of said translation lookaside buffer." Therefore, the Office Action does not show a teaching of each and every element recited in Claim 35.

The Applicants respectfully submit that because of the foregoing reasons, Claim 35 contains patentable subject matter and should be allowed. As a result of providing the foregoing arguments with respect to independent Claim 35, the Applicants have not commented on the remarks made by the Examiner regarding dependent Claims 36-40 but reserve the right to do so in the future should the need arise. Since Claims 36-40 depend on allowable Claim 35, Applicants respectfully submit that Claims 36-40 are in condition for allowance. The Applicants respectfully request allowance of Claims 35-40.

NEW CLAIMS 41-44

The Applicants have added new Claims 41-44 as presented in the Listing of the Claims. Because of the Applicants' foregoing arguments regarding Claims 12, 16, and 18, for example, the Applicants respectfully submit that new Claims 41-44 contain patentable subject matter. The Applicants respectfully submit that the cited references do not teach the subject matter presented in Claims 41-44. Therefore, Claims 41-44 are in condition for allowance.

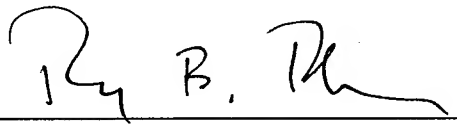
CONCLUSION

Based on at least the foregoing, the Applicants believe that Claims 12-44 are in condition for allowance. A Notice of Allowance is courteously solicited. Should anything remain in order to place the present application in condition for allowance, or should the Examiner disagree or have any question regarding this submission, the Examiner is kindly invited to contact the undersigned at (312) 775-8246.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: August 15, 2007

Respectfully submitted,



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